

A Short Length Low Complexity Low Delay Recursive LDPC Code

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Abstract: - Due to their low delay and complexity, short length codes are attractive for use in wireless communication systems. Also, achieving low complexity, high performance and low decoding latencies, is the key requirements of low-density parity-check (LDPC) code because these provide more reliable code for many applications. In this paper, a novel method was proposed to construct a short length code based on the convolutional encoder and LDPC decoder. In this code, delay and computational complexity of encoding and decoding were significantly reduced compared to other LDPC codes when they were simulated at the same length and code rate. The main contribution of this work was to design a code with low time delay and low computation complexity while having an improved bit error rate (BER) performance. Complexity and latency were reduced by using a convolutional technique for the encoding and by providing an improved parity-check matrix for the decoding. The codes were simulated over additive white Gaussian noise (AWGN) channel using different modulation schemes. Theoretical analysis denoted that the encoder and decoder may offer advantages in terms of latency and complexity, while simulation results have showed that the proposed code achieved an improvement over other LDPC codes that have the same length and code rates.

Key-Words: - LDPC codes, Low-density parity-check matrix (H), Convolutional encoder, Decoding complexity, Latency, BER performance.

1. Introduction

Low-density parity-check (LDPC) codes were investigated by Gallager [1]. With soft decoding algorithms on Tanner Graph, these codes can achieve outstanding capacity and approach Shannon limit over noisy channels at moderate decoding complexity [2]. The structure of the code is given by a parity-check matrix H , and different codes have different parity-check matrices [3]. LDPC codes are block codes and the biggest difference between them and classical block codes is how they are decoded. Due to high error correction performance, LDPC codes have become serious competitors to turbo codes [4], and they share the main concept of message passing algorithm as the turbo code. However, it is shown that the LDPC codes beat turbo codes in terms of bit error rate (BER) performance for the higher code rates [5,6]. Recently, many researchers have focused on performance analysis of recursive LDPC code. Based on the structure of the H matrix, a recursive can be designed using a set of shift-register where the encoder requires only a number of memory units. The recursive encoding significantly reduces the encoding time and the complexity compared to the encoding of LDPC

block codes [7]. It has been shown that the processing time (latency) and decoding complexity increase linearly with increasing code length. This means small length LDPC codes result in low computational complexity and low time delay. So, researchers in LDPC codes look for good code's performance, but they also look for code structures that allow reducing the hardware and software encoding and decoding complexity [8]. In more applications, it is desired to design a code with low complexity and latency where the decoding over the large code length would result in large latency and decoding complexity. In this work, it has been focused on a small code length to construct LDPC codes which can provide these requirements and have improved high BER performance. The convolutional encoder technique and LDPC decoder are utilized in this approach, where the proposed code is based on the convolutional encoder and LDPC decoder. This paper is organized as follows; an overview of LDPC code is described in section II, the convolutional encoder is reviewed in section III, the proposed model is detailed in section IV and simulation results are done in section VI.

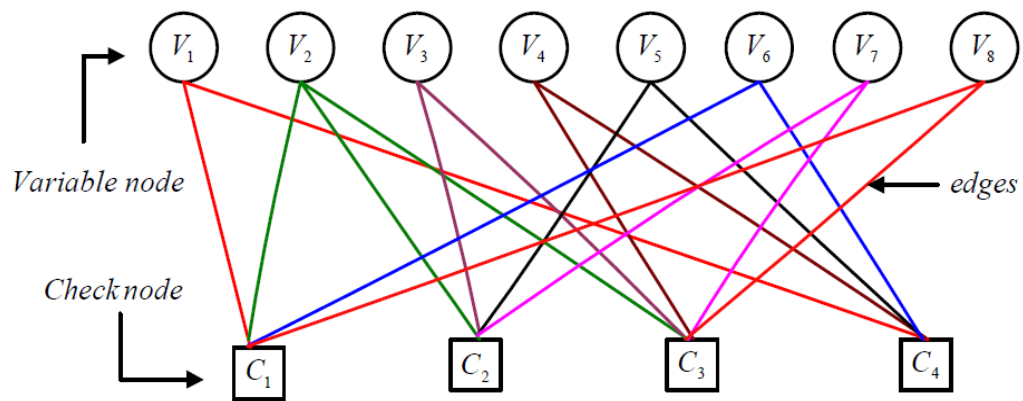


Fig.1. Tanner Graph Representations of LDPC code.

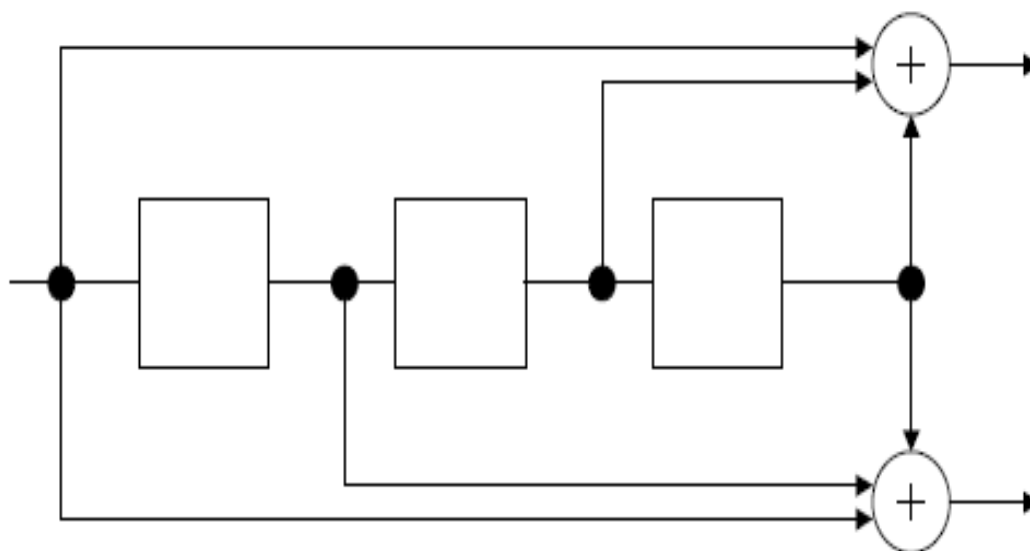


Fig.2. a model of convolutional encoder.

2. LDPC Code

The structure of the code is given by a parity-check matrix (H matrix). The code x is constructed so that $Hx^T = 0 \pmod{2}, \forall x \in c$

$$Hx^T = 0 \pmod{2}, \forall x \in c \quad (1)$$

The code may then be written as

$$x^T = [i \mid c] \quad (2)$$

Correspondingly, the parity check matrix may be split into two matrices:

$$H = [A \mid B] \quad (3)$$

Also, equation (1) may be written as

$$Ai + Bi = 0 \quad (4)$$

If the matrix B is non-singular, the code can be found as

$$c = B^{-1}Ai \quad (5)$$

H can be defined with parameters such as row weight (r_w) and column weight (c_w), where m and n represent the number of parity check equations and the code length respectively. The row weight corresponds to the number of non-zero elements in a row, while the column weight corresponds to the number of non-zero elements in a column. If the row weight and column weight are uniform with all the rows and columns, then LDPC codes are called regular LDPC codes. With the non-uniform row and column weights, the codes are called irregular codes [9]. The decoding of LDPC codes can be efficiently performed using Tanner graphs [3]. This graph is constructed from H matrix and contains two sets of nodes, variable nodes and parity nodes, which represent the n bits and parity constraints respectively. The number of edges in Tanner graph is equal to the number of ones in H matrix. Fig.1 shows the Tanner graph for the H matrix given below

$$H = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 1 & 0 & 0 \end{bmatrix} \quad (6)$$

The columns are represented as the variable node of set 8 and check node corresponding to the rows as the set of 4. As shown in Fig.1, H has a row weight of 4 and a column weight of 2.

Performance of LDPC codes is most related to the construction of H parameter which can be regular or irregular. The original LDPC codes presented by Gallager are regular and defined by a banded structure in H [10, 11]. There are three significant properties of H matrix: row-column (RC) constraints, girth, and rank. The RC constraints represent the weight of ones in rows and columns, the girth is the length of shortest cycles of Tanner graphs and the rank is the maximum number of linearly independent row vectors of the matrix. Increasing girth or column weight increases the minimum distance of the code and results in high BER performance [9]. The effect of girth on the performance of LDPC codes can be reduced by

choosing the codes having longer girths. Generally, short length LDPC codes require a longer girth for a good performance [12]. In the receiver, there are many algorithms known to recover information [12], such as; 1) sum-product algorithm (SPA), 2) min-sum algorithm, 3) min-max algorithm, 4) message-passing algorithm and 5) bit-flipping decoding algorithm. The SPA is based on belief propagation and has the best decoding performance but with high computational complexity. In this paper, all simulation results are obtained using the sum-product algorithm.

3. An overview of the convolutional encoder

In this code, the bits come in serial form instead of a block form. Convolutional codes are commonly specified by three parameters (n , k , and K) where these parameters correspond to the number of output bits, the number of input bits and the length constraint respectively. These codes can be recursive or non-recursive, systematic or non-systematic. If input data appear in the code, the convolutional code is said to be systematic code. Convolutional encoder consists of an M-stage shift register and multiplexers. Fig.2 shows an example for (2,1,4) convolutional encoder with a code rate $R=1/2$. The block diagram shows a model of a non-recursive, systematic convolutional encoder.

The impulse response streams $g_1(n)$ and $g_2(n)$ for the input $x(n) = (1\ 0\ 0\ 0\ \dots)$ for the encoder shown in Fig.2 can be introduced as follows:

$$g_1(n) = x(n) + x(n-2) + x(n-3) \quad (7)$$

$$g_2(n) = x(n) + x(n-1) + x(n-3) \quad (8)$$

Impulse responses can be written in a sequence form as $g_1 = [1011]$ and $g_2 = [1101]$, or in an octal form as $g_1 = 13$ and $g_2 = 15$. In addition, they can be defined in a polynomial form as

$$g_1(D) = 1 + D^2 + D^3 \quad (9)$$

$$g_2(D) = 1 + D + D^3 \quad (10)$$

where D is an operator related to the Z-transform. The linear combination of the two sequences can be described as

$$G_i = [g_1(D) \ g_2(D)] \quad 0 \leq i \leq r \quad (11)$$

The generator matrix of the convolutional encoder can be described in a matrix form as

$$G = \begin{bmatrix} G_0 & G_1 & G_2 & \dots & G_r & 0 & 0 \\ & G_0 & G_1 & G_2 & \dots & G_r & 0 \\ & & G_0 & G_1 & G_2 & \dots & G_r & \dots \\ & & & \vdots & & & & \end{bmatrix} \quad (12)$$

Then, the transform of the encoder output can be expressed as

$$Y(D) = X(D) G(D) \quad (13)$$

where $X(D)$ is the input sequence and

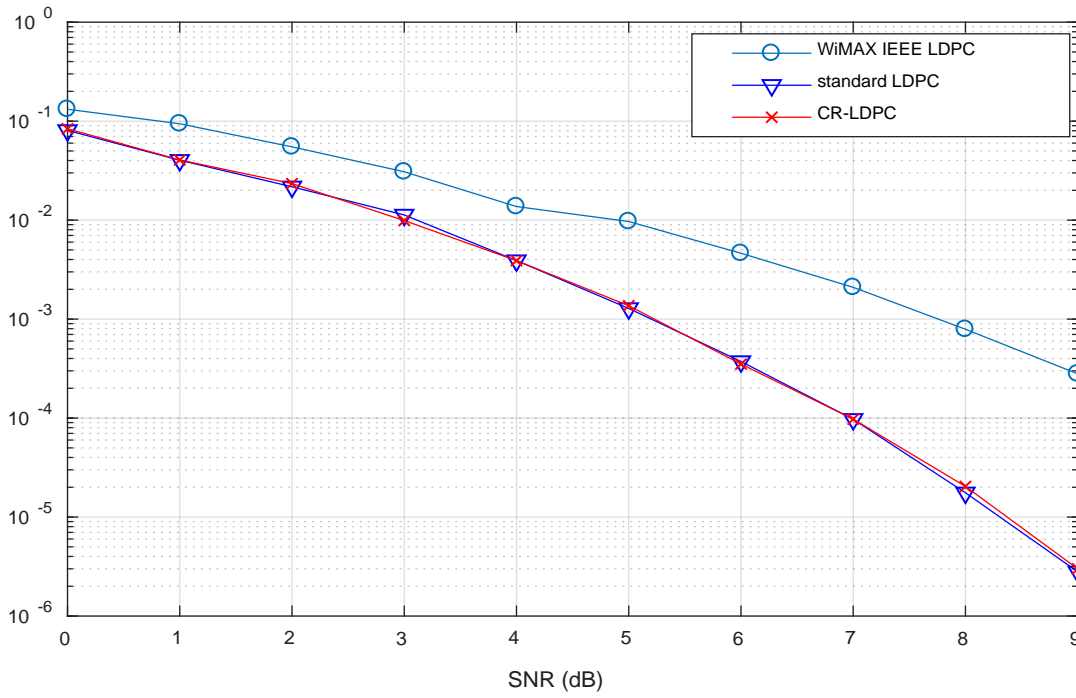


Fig.6 Performance of CR-LDPC, LDPC standard, and WiMAX LDPC codes, R=1/2, QPSK

$$Y(D) = [Y_1(D) Y_2(D)] \quad (14)$$

For $g_1 = [1011]$ and $g_2 = [1101]$, the generator matrix is

$$G = \begin{bmatrix} 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 0 & 1 & 1 \\ & & & & \vdots & & & & \end{bmatrix} \quad (15)$$

If data sequence $u = [u_0 u_1 \dots u_m]$, then block code can be found as

$$c = u G \quad (16)$$

To confirm a better degree distribution of ones and girth, and then provides improved BER performance, the length of the generator r must be selected so that it is no less than $k/2$, as will be shown in the next sections.

4. System Model

In communication systems, low BER of LDPC code is a necessary but not a sufficient requirement. The latency (time required for encoding and decoding) and complexity of the encoder and decoder also needed to be considered. Recently, a lot of research has been done to present a high BER performance LDPC code with low latency and complexity. In [13-16], the researchers propose several methods to reduce the decoding complexity by updating the individual decoder algorithm or by reducing the total global wire-length. While achieving short length LDPC codes with low delay and complexity remains a challenge. In general, complexity and delay are directly related to the following issues; the number of operations required in each node, the average number of iterations, and the number of active nodes in each iteration [17]. The model proposed attempts to reduce delay and complexity of the encoder by replacing the LDPC block encoding with only a set of the shift register, and reduce delay and complexity of the decoder by constructing a novel parity-check matrix which has an improved construction that can decode the information with low delay and complexity as well as with optimum BER performance. The code generated based on convolutional encoding and recursive parity-check matrix, thus named CR-LDPC code. The two following sections show how encoder and decoder are constructed.

4.1 Encoder Construction

Here, an attempt has been made to construct a recursive and systematic encoder. The recursive encoding means that the encoder repeats the encoding procedure after a specific length of information. The code is systematic in that, the data bits are part of the code and the parity-check matrix is a repeat-accumulate matrix similar to the matrix of standard WiMAX code [17]. These considerations simplify the hardware implementation and allow the code to be easily encoded and decoded. In the

convolutional encoder, the code is generated using a set of shift registers which are implemented according to the generator sequence. Generator sequence is a key parameter of the proposed code since it specifies the configuration of the encoder and the decoder. The block diagram depicted in Fig.3 shows the simplest way to generate CR-LDPC code. Firstly, the information is encoded into two pairs of the parity bit, and secondly, the information is added at the end of the code by the multiplexer. The memory unit is only used to illustrate that the information is separated from the parity bits and the code generated is similar to the WiMAX LDPC code.

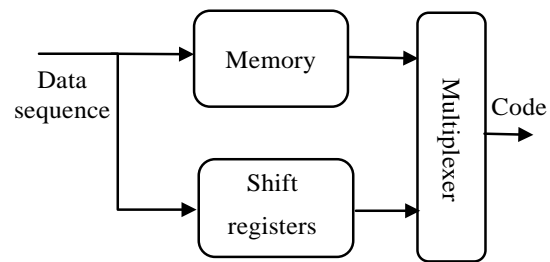


Fig.3 the block diagram of CR-LDPC

In addition to data bits, a sequence of zero bits of length L_i is added at the end of the information and provided as input to the shift registers. This addition shifts data sequence by L_i times and increases the parity sequence from k to $k+L_i$, where k is the size of information bits. The most important benefit of adding zero bits is that it allows for providing a code with variable lengths and multi-rates. As a result, parity bits are produced separately from information using a convolutional encoder, and then the information is added at the end of parity bits to perform the CR-LDPC code. Fig.2 shows a convolutional encoder of $(2,1,4)$; however, CR-LDPC encoder requires a convolutional encoder of one input and one output, such encoder has a rate of one and can be defined by a single generator polynomial. The generator matrix for the proposed encoder can be obtained as follows.

Consider an encoder with a generator polynomial of $g = [g_1 g_2 \dots g_r]$. The generator matrix of convolutional encoder can be found using equation (12)

$$G_c = \begin{bmatrix} g_0 & g_1 & g_2 & \dots & g_r & 0 & 0 \\ 0 & g_0 & g_1 & g_2 & \dots & g_r & 0 & \dots \\ 0 & 0 & g_0 & g_1 & g_2 & \dots & g_r & \dots \\ & & & \vdots & & & & \end{bmatrix} \quad (17)$$

For inputs of k data bits and L_i zero bits, the equivalent generator matrix is

$$G_e = \begin{bmatrix} 1 & 0 & 0 & g_0 & g_1 & g_2 & \dots & g_r & 0 & 0 \\ 0 & 1 & 0 & 0 & g_0 & g_1 & g_2 & \dots & g_r & 0 & \dots \\ 0 & 0 & 1 & 0 & 0 & g_0 & g_1 & g_2 & \dots & g_r & \dots \\ & & & & \vdots & & & & & & \end{bmatrix} \quad (18)$$

This equation can be written as

$$G_e = M[L_i + k, 2(L_i + k)] \quad (19)$$

The information is not sent with code, then the actual generator matrix of the CR - LDPC encoder can be expressed as

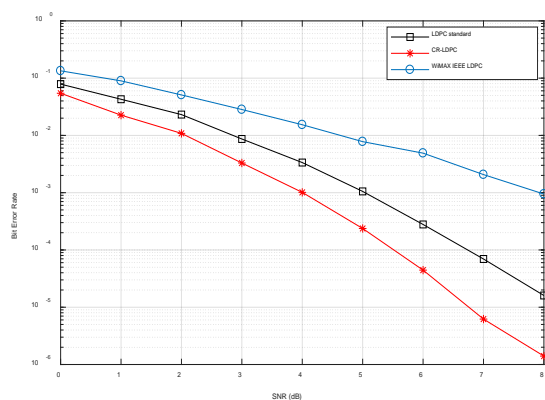


Fig.7 Performance of CR-LDPC, LDPC standard, and WiMAX LDPC codes, $L_i=4$, QPSK

Fig.8 shows results when $k=12$, $L_i=12$, and all codes having a rate of $1/3$. The curves show that the BER performance of CR-LDPC code is better than standard LDPC code and WiMAX LDPC code despite the length of WiMAX LDPC code is 48 bits.

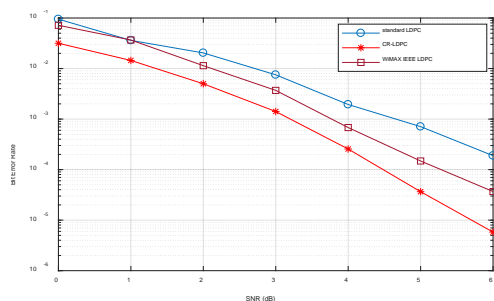


Fig.8 Performance of CR-LDPC, standard LDPC, and WiMAX LDPC codes, $R=1/3$, QPSK

There are several factors behind this significant improvement in the BER performance: 1) the proposed code has a large minimum distance. 2) the constructed parity-check matrix has good randomness and irregular construction. 3) the Tanner graph is characterized by a large girth. 4) the zero inputs inserted at the decoder significantly increase the SNR of the received code, as they represent a received message with no error probability. 5) By the process of adding zeroes, variable nodes that have a low number of edges are avoided 6) the decoder uses a matrix of size (24×48) instead of (24×36) , this leads to a better decoding performance because the performance of LDPC decoder directly relates to the size of parity-check matrix. The BER performance over 8PSK using same parameters is depicted in Fig.9. As in LDPC block code, the performance of CR-LDPC is improved when code length is increased.

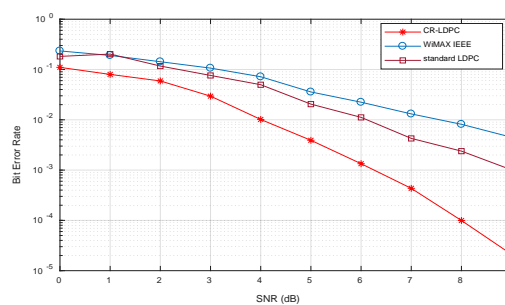


Fig.9 Performance of CR-LDPC, LDPC standard, and WiMAX LDPC codes, $R=1/3$, 8PSK

Fig.10 shows results when data length and code rate are set to 24 bits and $1/2$ respectively. The generator sequence is $g = 6111$ and $L_i=0$. Again, using $L_i=4$ bits, the performance of the proposed code is significantly increased as shown in Fig.11.

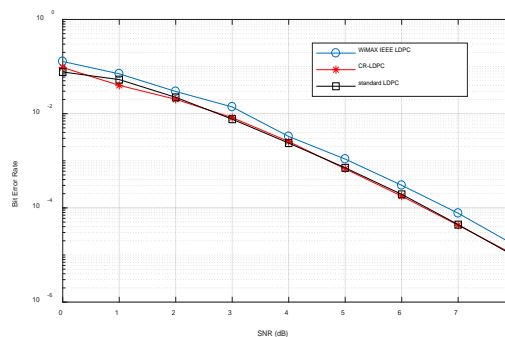


Fig.10 Performance of CR-LDPC, LDPC standard, and WiMAX LDPC codes, $R=1/2$, QPSK

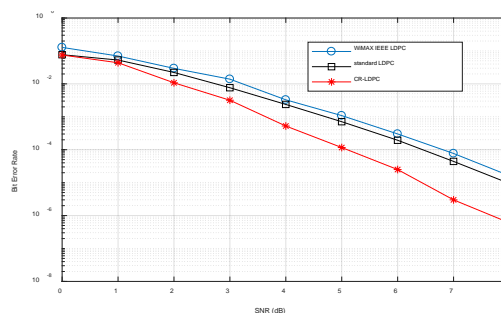


Fig.11 Performance of CR-LDPC, LDPC standard, and WiMAX LDPC codes, $L_i=4$, QPSK

6. Conclusion

In this paper, a novel short length LDPC code is presented, called convolutional recursive LDPC (CR-LDPC) code. This code was based on convolutional encoding and LDPC decoding. The parity-check matrix used in the decoder was derived from the generator matrix of the convolutional encoder. Several constraints were considered through designing the generator matrix at the encoder in order to make the parity-check matrix simple and efficient. It has been analytically demonstrated that the proposed structure can significantly reduce

computational complexity and delay of encoding by using a convolutional encoder instead of using LDPC block encoder. While delay and complexity of the decoder were reduced by constructing an improved generator matrix so that the parity-check matrix constructed can achieve these requirements. By comparing results with WiMAX LDPC codes and LDPC codes which based on a block encoding method, simulation results showed that the proposed code achieved a suitable performance at rate 1/2, and a good performance when the code rate changed to 1/3.

References:

- [1] R. G. Gallager, "Low-Density Parity-Check Codes," Cambridge, Massachusetts: M.I.T. Press, 1963.
- [2] J. Cui, Y. Wang, and H. Yu, "Systematic Construction and Verification Methodology for LDPC Codes," Department of Electrical Engineering, Tong University, Shanghai Jiao, China.
- [3] K. Fagervik and A. S. Larssen, "Performance and Complexity Comparison of Low-density Parity Check Codes and Turbo Codes," Stavanger University College, Stavanger University College.
- [4] N. Hassan, M. Lentmaier, and G. P. Fettweis, "Comparison of LDPC Block and LDPC Convolutional Codes Based on their Decoding Latency," *7th International Symposium on Turbo Codes & related Topics (ISTC 2012)*, Gotheburg, Schweden, August, 2012, pp. 27-31.
- [5] M. D., A. A. Elazm and M. Shokair, "Evaluation of Complexity Versus Performance for Turbo Code and LDPC Under Different Code Rates," *The Fourth International Conference on Advances in Satellite and Space Communications, SPACOMM*, 2012.
- [6] K. Narwal, Y. Sharma, "Performance Comparison of Turbo Codes with other Forward Error Correcting Codes," *International Journal of Electronics and Computer Science Engineering, IJECSE*, vol. 1, no. 2.
- [7] Z. Si, S. Wang, and J. Ma, "An Efficient Method to Construct Parity-Check Matrices for Recursively Encoding Spatially Coupled LDPC Codes," *Extension of the paper published in the 2015 IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, Hong Kong, China, 30 August–2 September 2015., August 2016.
- [8] C. D. García, "Search for Improvements in Low-density Parity Check Codes for WiMAX (802.16e) Applications," Politecnico Di Torino, Ms. Thesis, 2014.
- [9] J. Maier, "Studies on Various Algorithmic improvement in non-Binary LDPC Decoder Design," Anna University, Ph.D. Thesis, October 2015.
- [10] Xiao-Yu Hu, E. Eleftheriou, and D. M. Arnold, "Regular and Irregular Progressive Edge-Growth," IBM Research.
- [11] S. J. Johnson, "Introducing Low-Density Parity-Check Codes," Institute for Information Transmission (LIT), School of Electrical Engineering and Computer Science, The University of Newcastle, Australia.
- [12] K. Deergha Rao, "Channel Coding Techniques for Wireless Communications," Springer India, 2015.
- [13] K. Fagervik, A. S. Larssen, P. Pattisapu, and P. K. Bora, "Reduced Complexity LDPC Decoding using Forced Convergence," Dresden University of Technology, Vodafone Chair Mobile Communications Systems D-01062 Dresden, Germany.
- [14] T. Mohsenin, D. N. Truong, and B. M. Baas, "A Low-Complexity Message-Passing Algorithm for Reduced Routing Congestion in LDPC Decoders," *IEEE Transaction on Circuits and Systems*, vol. 57, no.5, May. 2010, pp. 1048-1060.
- [15] Darabiha, "Block-Interlaced LDPC Decoders with Reduced Interconnect Complexity," *IEEE Transaction on Circuits and Systems*, vol. 55, no.1, January. 2008, 74-78.
- [16] J. Chen, "Reduced-Complexity Decoding of LDPC Codes," *IEEE Transaction on Communication*, vol. 53, No. 8, August. 2005, pp. 1288-1298
- [17] K. Fagervik, A. S. Larssen, P. Pattisapu and P. K. Bora, "Reduced Complexity LDPC Decoding using Forced Convergence," Dresden University of Technology, Vodafone Chair Mobile Communications Systems D-01062 Dresden, Germany.
- [18] T. Brack, M. Alles, F. Kienle and N. When, "A SYNTHESIZABLE IP CORE FOR WIMAX 802.16E LDPC CODE DECODING," *The 17th Annual IEEE International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC'06)*. October 2006.